negligible. Because of this large effect of reverse feedback on the value of the input impedance, more accurate circuit design results should be obtained using the model based upon G_{ME}.

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Broad-Band Internal Matching of Microwave Power GaAs MESFET's

KAZUHIKO HONJO, YOICHIRO TAKAYAMA, AND ASAMITSU HIGASHISAKA

Abstract—**Broad-band internal matching techniques for high-power GaAs MESFET's at *C* band have been developed, adopting novel circuit configurations and large-signal characterizations in the circuit design. The lumped-element two-section input matching network is formed on a single ceramic plate with a high dielectric constant. The semidistributed single-section output circuit is formed in microstrip pattern on an alumina plate. The internally matched GaAs FET with 11 200-μm total gate width developed has a 2.5-W power output at 1-dB gain compression and a 4.4-W saturated power output with 5.5-dB linear gain from 4.2 to 7.2 GHz without external matching. The FET internally matched from 4.5 to 6.5 GHz exhibited 5-W saturated power output with 6-dB linear gain.**

I. Introduction

HIGH-POWER GaAs FET's, exhibiting significant progress in recent years, are realized basically by increasing the total gate width as well as the drain-source breakdown voltage. As a result, the device input impedance decreases steadily in proportion to the total gate width. Thus the maximum attainable power and gain degenerate by matching limitations and losses resulting from the interposition of fixed parasitic elements in the device–circuit interface. To solve such matching limitations and exhibit the basic device capabilities, the introduction of so-called internal matching networks (IMN) close to active device on the carrier or package is a natural consequence. The fixed parasitic elements constrain redundant design, which degrades device broad-band characteristics and brings extra loss.

Internal matching is standard technique for high-power bipolar transistors for use below 5 GHz [1]. With respect to the power GaAs FET of higher frequency capabilities, compared with the bipolar transistors, refined techniques effective at frequencies above 5 GHz are required [2]. In such frequency ranges, input and output phase uniformity within multicell or multichip devices and circuit losses become much more significant.

The purpose of this paper is to present broad-band internal matching techniques for high-power GaAs MESFET's at *C* band [3], adopting novel circuit configurations, where the two-section input matching network is formed on a single thin ceramic plate with a high dielectric constant and large-signal characterizations in the circuit design. The matching circuit losses are also analyzed to obtain a basic understanding of the effect on matching limitations. The internally matched GaAs FET with 11 200-μm total gate width has a 2.5-W power output at 1-dB gain compression and a 4.4-W saturated power output with a linear gain of 5.5 dB from 4.2 to 7.2 GHz without external matching. A 5-W maximum saturated power output has also been measured with narrow-band-width design over the 4.5–6.5-GHz frequency range.

II. Internal Matching Network Design

For broad-band high-power output performance of power GaAs FET's, large-signal techniques as well as small-signal ones are introduced for the matching network design. In the grounded source configuration, GaAs MESFET optimum power load impedance, by which the maximum power output can be drawn, shifts significantly as a function of input drive level. However, there is little variation in the input impedance. Therefore, large-signal matching is required mainly for the output network, as a first-order consideration.

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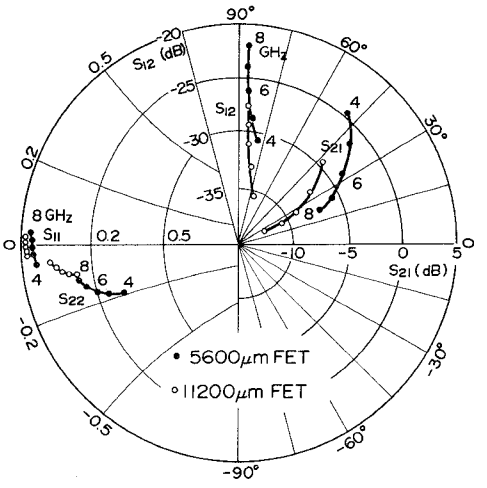


Fig. 1. Small-signal S parameters for GaAs MESFET's with 5600- and 11 200-μm gate widths.

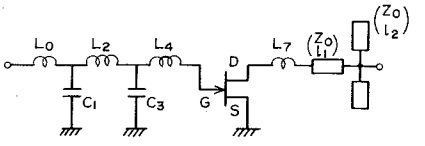


Fig. 2. Equivalent circuit of internal matching network.

The small-signal S parameters of GaAs FET's with single- and two-chip structures are shown in Fig. 1. Their total gate widths are 5600 and 11 200 μm, respectively. The single-chip GaAs MESFET has a two-cell structure which has 56 parallel gates with 4 gate bonding pads and 4 drain pads [2]. Gate length is 1.3 μm and total gate width is 5600 μm. The single-chip measures 1.5×0.65 mm. To reduce bonding wire inductance for source grounding, the source electrode is grounded by thin metal films evaporated on the device periphery without bonding wires.

The equivalent circuit of the internal matching network is shown in Fig. 2. Input internal matching networks of the lumped-element two-section low-pass type were designed, as shown in the figure. Starting element values for the input networks before computer optimization were determined by defining a Chebyshev impedance-matching network of low-pass filter form from Matthaei's work [6].

Output internal matching networks of the one-section semidistributed form were designed with microstrip structure. The output networks were determined to achieve high-power output and flat output saturation power level over the design frequency range. The variation in optimum power load impedance was predicted, based on the small-signal output-impedance and static drain–voltage source–current characteristics. Large-signal matching was attempted by considering the increase of the optimum power load conductance of the FET's with the increase in input power drive level [4].

Based on the initial circuit element values and S parameters, detailed fitting to device design circuit parameters was performed by a computer-aided design optimization program. Then, matching networks having prototype output matching networks were designed and fabricated. In Fig. 2, the designed values of the 5600-μm FET internal matching network elements are $L_0 = 0.2$ nH, $C_1 = 1.46$ pF, $L_2 = 0.495$ nH, $C_3 = 6.18$ pF, $L_4 = 0.139$ nH, $L_7 = 0.1$ nH, $Z_0 = 50\ \Omega$, $l_1 = 1.5$ mm, and $l_2 = 2.25$ mm, and those of the 11 200-μm FET internal matching network elements are $L_0 = 0.1$ nH, $C_1 = 1.49$ pF, $L_2 = 0.479$ nH, $C_3 = 8.60$ pF, $L_4 = 0.077$ nH, $L_7 = 0.096$ nH, $Z_0 = 50\ \Omega$, $l_1 = 1.15$ mm, and $l_2 = 2.5$ mm. Finally, with the equivalent load-pull measurements, whose method was developed for broad-band power transistor load-pull characterization in the NEC laboratory [5], the output internal matching networks were experimentally optimized to obtain high-power output over the design frequency range by adjusting the microstrip pattern.

III. Circuit Configuration

In this section, capacitors and inductors for the internal matching networks are discussed and a novel circuit configuration is described. The two-section input matching network is formed on a single ceramic plate with a high dielectric constant, and a one-section distributed output matching network is formed on an alumina ceramic plate. This made possible low-cost fabrications as well as high-power broad-band matching.

A. Capacitors

Capacitors for the internal matching networks must have small parasitic inductance, small resistance, dimensions easy to deal with, sufficient thermal and mechanical strength, small temperature coefficient, over 40-V breakdown voltage, and low cost. MOS, metal–insulator–semiconductor (MIS), and metal–insulator–metal (MIM) capacitors are available for the internal matching networks. MOS and MIS capacitors have large series resistance compared with MIM capacitors, because of the utilization of highly doped silicon substrates for forming electrodes for MOS and MIS capacitors. As a result, MIM capacitors with appropriate dielectric material are considered to be most suitable for internal matching networks [2].

The dielectric material used for the capacitors is low-loss ceramic of unloaded $Q \simeq 7000$ at 7 GHz, whose main composition is B_aO–T_iO_2 with a relative dielectric constant ϵ_r of 39.5 and 0.1-mm thickness. All capacitors in the input internal matching network were formed on a single ceramic plate. Distances between the capacitors were determined according to the bonding wire length required to realize the given inductances. To maintain the capacitor as a lumped element and to achieve phase uniformity, large capacitors were subdivided. Location of all input circuit capacitors on a single ceramic plate makes it easy to assemble them on a carrier.

B. Inductors

Thirty-μm-diameter Au bonding wires were used for the inductors. In the internal matching networks, since these wires are located partially above capacitor electrodes,

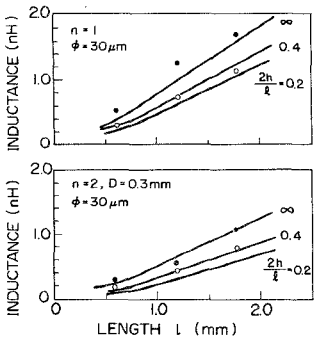
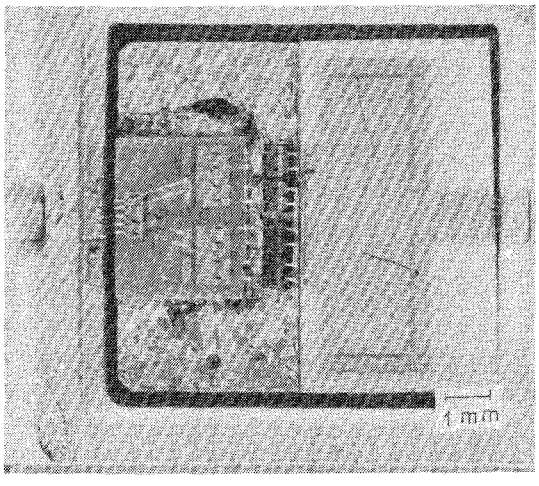
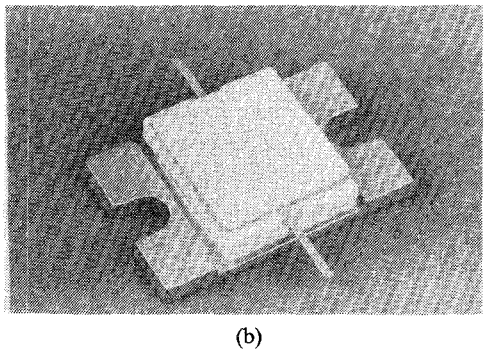


Fig. 3. Calculated values and measured values of wire inductors (n = number of wires, ϕ = diameter of a wire, D = distance from one another, h = height above ground).



(a)



(b)

Fig. 4. Photograph of 11 200-μm gate width FET's with IMN (a) and a T-10 case (b).

inductance values are affected by the electrodes. The bonding wires are, also, mutually coupled. Thus the inductance values were predicted from calculated values which describe the inductances of the grounded straight round wires in parallel [7], and the practical inductance values were found experimentally by preliminary measurement of the wires bonded on test circuit carriers. Fig. 3 shows the calculated values and the experimental values of the inductance. In the figure, the filled circles show the experimental values measured on a 1-mm thick alumina plate, and the circles show the experimental values measured on a grounded metal plate at 6 GHz, and the lines show the calculated values.

The found length and number of the wires for the 5600-μm FET are 840 μm$\times$4 for L_0, 1270 μm$\times$2 for L_2, 1200 μm$\times$4 for L_4, and 350 μm$\times$4 for L_7, and those for the 11 200-μm FET are 360 μm$\times$4 for L_0, 2050 μm$\times$4 for L_2, 1130 μm$\times$8 for L_4, and 710 μm$\times$8 for L_7.

C. Circuit Fabrication

A photograph of the two-chip GaAs FET (11 200-μm total gate width) with the internal matching network is shown in Fig. 4(a). The input matching network of lumped elements consists of parallel capacitors on a single ceramic plate 0.1-mm-thick and 30-μm-diameter bonding wires. The thin ceramic substrate and FET chips are mounted on a metal ridge. The output circuit consists of bonding wires and parallel microstrip stubs formed on a 1-mm-thick alumina ceramic substrate. This semidistributed realization simplified the output circuit adjusting and assembly process. Input and output terminals are composed of 50-Ω microstriplines.

The 11 200-μm total gate width internally matched two-chip FET is assembled in a T-10 case developed for power GaAs FET's. Fig. 4(b) shows the T-10 case.

IV. Performance

Microwave performance for internally matched single-chip FET of 5600-μm total gate width and two-chip FET of 11 200-μm total gate width are described in this section. These internally matched FET's are designed for 5–7-GHz amplifiers.

A. Internally Matched FET with 5600-μm Gate Width

The small- and large-signal input impedance are shown in Fig. 5. The small-signal output impedance and large-signal optimum power load impedances are shown in Fig. 6. In the figures, the filled circles show small-signal impedances, and triangles and squares indicate large-signal input impedance, and optimum power load impedances in large-signal operation under several input power levels, measured with the equivalent load-pull method.

Small-signal optimum power load impedance is the complex conjugate of the small-signal output impedance. It is seen that the input impedance variation is small, compared with the output optimum power load impedance variation with the increase in input power levels. The higher the input drive level becomes, the closer to 50 Ω the optimum power load-impedance becomes. It is also seen that the higher the operating frequency becomes (5, 6, and 7 GHz), the closer to 50 Ω the optimum load impedances become, near the saturation level denoted by notation D(+27 dBm IN). These characteristics compensate for the frequency dependence of FET saturated power level.

The power output response versus frequency and input–output response of the internally matched FET with 5600-μm gate width, without any external matching, are shown in Figs. 7 and 8, respectively. The internally matched FET has a 1.5-W power output at 1-dB gain compression with a linear gain of 6.5 $\pm$ 1.5 dB from 4.6 to 7.6 GHz, and 2.6-W saturated power output and 24-percent maximum power added efficiency, as shown in the

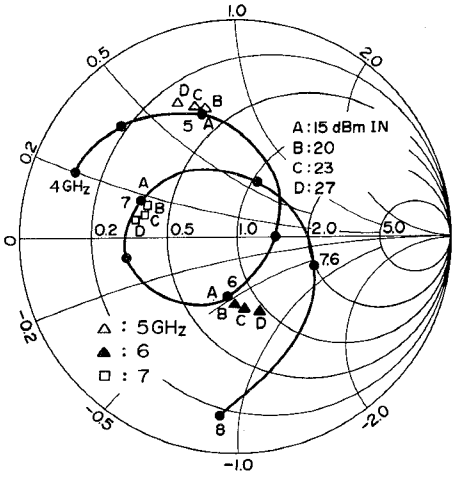


Fig. 5. Small-signal and large-signal input impedance of the internally matched FET with 5600-μm gate width.

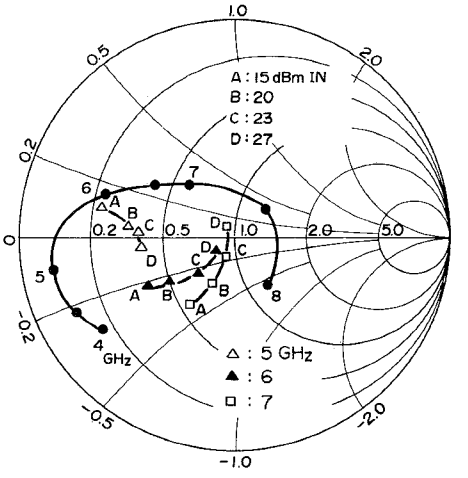


Fig. 6. Small-signal output impedance and large-signal optimum power load impedances of internally matched FET with 5600-μm gate width.

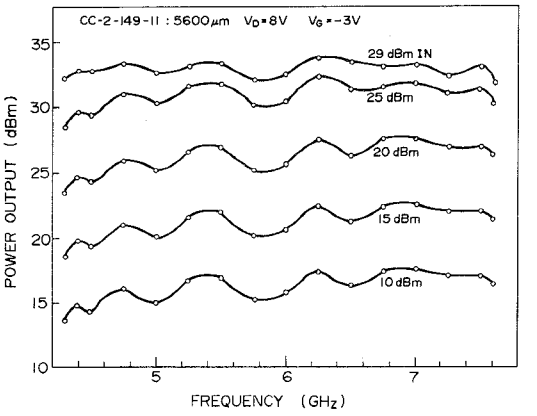


Fig. 7. Output power response versus frequency of internally matched FET with 5600-μm width, measured without any external matching.

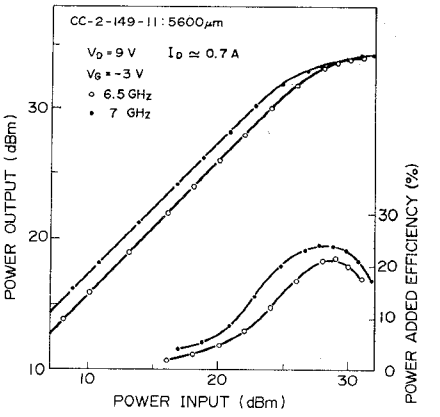


Fig. 8. Input–output response of internally matched FET with 5600-μm gate width, measured without any external matching.

figures. Third-order intermodulation product C/I measured at 6 GHz with the signals separated 10 MHz and 27-dBm total power output was 48 dB.

B. Internally Matched FET with 11 200-μm Gate Width

The power output response versus frequency and the typical input–output response of the internally matched FET with two-chip 11 200-μm total gate width without external matching are shown in Figs. 9 and 10, respectively. The internally matched FET has a 2.5-W power output at 1-dB gain compression with a linear gain of 5.5 $\pm$ 1.5 dB from 4.2 to 7.2 GHz and 4.4-W saturated power output and 20-percent maximum power added efficiency. Matching over the narrow bandwidth, maximum saturated power output of 5 W was achieved with a linear gain of 6 dB from 4.5 to 6.5 GHz.

V. Circuit Loss Considerations

This section reports results of the investigation on internal matching circuit losses, which limit broad-band high-power matching of low-impedance power GaAs FET's.

The most significant loss elements for lumped inductors and capacitors, used as internal matching elements, are resistive losses in the conductive bonding wires and electrodes, respectively, caused by the skin effect. In the case that the length of a wire is much longer than the diameter of a wire, the inductance value is in proportion to wire length, as shown in Fig. 3. Therefore, a quality factor for the inductor is represented as follows:

$$Q_I = \frac{\omega L}{R_I} = \alpha_I \omega^{1/2} \tag{1}$$

and, assuming that capacitor length of propagation direction is constant and capacity is controlled by width of a capacitor, a quality factor for capacitor is represented as follows [8]:

$$Q_c = \frac{1}{\omega C R_c} = \alpha_c \omega^{-3/2} \tag{2}$$

where α_I, for equal diameter wires of the same material, is independent of wire length, and α_C, for equal thickness capacitor of the same material, is independent of the electrode area.

Constants α_I and α_C were obtained from measurements in the C band. In the analysis, the value of $Q_I = 50$–80 and $Q_C = 30$–60 at 6 GHz were used.

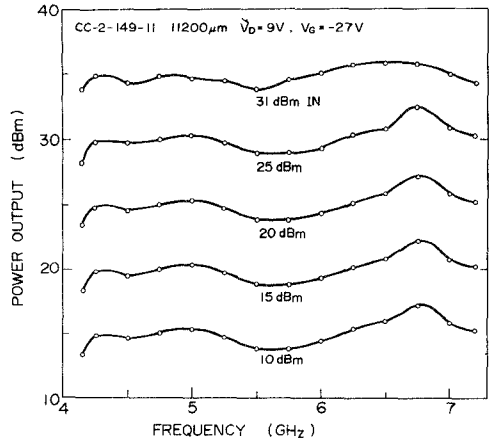


Fig. 9. Output power response versus frequency of internally matched FET with 11 200-μm gate width, measured without any external matching.

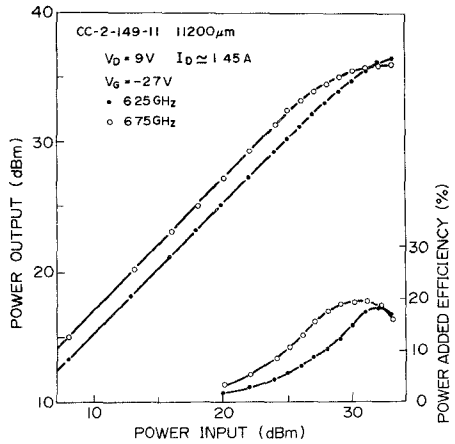


Fig. 10. Input–output response of internally matched FET with 11 200-μm gate width, measured without external matching.

The main loss for microstrip circuits, formed with Cr–Au metal conductor system on 1-mm-thick alumina substrate, is microstrip resistive loss caused by the skin effect. The quality factor is $Q_M = 150 \sim 250$. The propagation constant is given as

$$\gamma = \beta\left(\frac{1}{2Q_M} + j\right) \tag{3}$$

where β is phase constant. Introducing the loss elements expressed by (1), (2), and (3), the circuit losses were analyzed.

First, to obtain a fundamental understanding of matching network losses, lumped-element low-pass-type Chebyshev impedance-matching networks with pure resistive load were investigated. The circuit losses of a two-section matching network in which the return losses are not included, as a function of frequency for several load resistances, are shown in Fig. 11. The input source impedance is 50 Ω in all cases. The lower the load resistance becomes, the larger the circuit loss is, especially at higher frequencies. The loss abruptly increases in a higher frequency range of over the center frequency 6 GHz. The reason for this is the frequency dependence of Q_C decreasing as $\omega^{-3/2}$. Therefore, realization of high-Q capacitors is one of the most important matters for broad-band and high-power matching networks. Fig. 12 compares the total loss of a two-element matching circuit with the total loss of a four-element circuit and that of a six-element circuit.

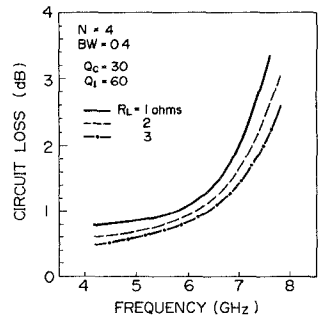


Fig. 11. Circuit losses of two-section matching network as a function of frequency for several load resistances for 50-Ω input source impedance. N is number of reactive elements.

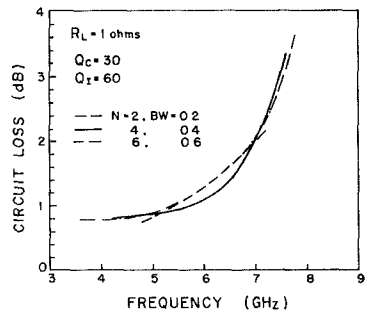


Fig. 12. Circuit loss dependence on matching section number.

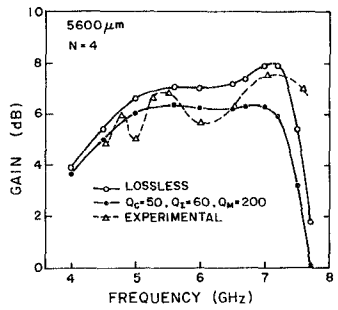


Fig. 13. Experimental small-signal gain response of internally matched 5600-μm FET and calculated values, including circuit losses.

It is seen that the loss is nearly independent of reactive element number N. Here, BW is the fractional bandwidth.

The calculated small-signal gain responses of the internally matched FET with 5600-μm gate width are shown in Fig. 13, compared with the experimental response.

VI. Conclusions

Broad-band internal matching techniques for high-power GaAs MESFET's for use in the C band have been developed. Novel circuit configurations and large-signal characteizations were adopted in the circuit design. The lumped element two-section input matching network is formed on a single ceramic plate with a relative dielectric

constant of 39.5. The single-section output matching network is formed in microstrip pattern on a 1-mm-thick alumina ceramic plate.

To obtain a basic understanding of circuit loss effects on low-impedance broad-band matching, matching circuit losses were analyzed and the results were presented.

The internally matched GaAs FET developed has a 2.5-W power output at 1-dB gain compression and a 4.4-W saturated power output with 5.5-dB linear gain from 4.2 to 7.2 GHz without external matching. The GaAs FET internally matched over the narrow band exhibited 5-W saturated power output with a linear gain of 6 dB from 4.5 to 6.5 GHz.

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Design Theory for Broad-Band YIG-Tuned FET Oscillators

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***Abstract*—Design techniques that have been successfully used on the development of *X*-band GaAs FET YIG-tuned oscillators are presented. The design procedure results in the maximization of the oscillator bandwidth. Small-signal device characterization is utilized and accurately predicts the oscillator bandwidth. Spurious oscillation conditions are discussed, and design techniques are prescribed for eliminating spurious oscillations in both the active circuit and resonator. The operation of an experimental oscillator verifies the design procedure.**

I. INTRODUCTION

As GaAs FET technology matures circuit designers are looking to these devices for an increasing variety of applications. The high-frequency performance of FET's coupled with their high-efficiency potential make them attractive competitors to the more established solid-state components such as bulk-effect devices and bipolar transistors for use as fundamental signal sources.

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To date there have been relatively few reports in the literature on FET oscillator development. Most of the early reports were concerned with units characterized by relatively narrow bandwidths of a few percent [1]–[5]. More recent reports [6]–[8] establish the potential of the GaAs FET for use as broad-band fundamental signal sources but do not give detailed accounts of the design techniques used.

This paper presents circuit design techniques that have been used successfully in the design of *X*-band YIG-tuned oscillators. The design techniques result in maximization of the oscillator bandwidth. The circuit analysis also yields information on possible spurious oscillation conditions and their elimination. The operation of an experimental oscillator verifies the design predictions.

II. DESIGN TECHNIQUES

The design approach involves a computer model investigation of the interface between the device and feedback circuit and the microwave resonator, in this case a

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